

TO: Distribution

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SUBJECT: Operation With Varying Multics Configurations

MULTICS
File

Operation of Multics with large configurations requires some changes to operational procedures. In order to minimize the confusion when changing configurations, changes to operational procedures have been made that will apply to any configurations. Remaining configuration dependent considerations are specifically noted. The following is to be used for all configuration:

I. Switch settings

a. Memory controller

- i) The PORT ENABLE switches for all memory controllers using Multics (including the development machine) should be set in the "MASK", i.e., "IN LINE", position for all ports. The objective is that these switches should never have to be changed when changing configuration.

Note: Due to a design inconsistency, if "memory G" is changed from one GIOC to the other, this memory must be initialized (at the memory maintenance panel) before bootloading.

- ii) The CONTROL PROCESSOR switch should be set as follows. The first memory (in the BOS deck) is set to the first CPU (in the BOS deck), the second memory to the second CPU, etc. When there are more memories than CPU's, then all memories not matched to a CPU's (as just described) are set for the last CPU in the BOS deck.

- b. Processor - all switches except the CPU NO must be identical for all processors in Multics. The port enable switches for unused memories is to be set to "OFF".

The EXECUTE button is used to force the processor to enter BOS.

This can be done in one of two ways:

- i) Usually BOS will be entered by causing an execute fault.

For this to occur the EXECUTE SWITCHES switch must be down when the EXECUTE button is pressed. The switch should normally be left in the down position. DO NOT put the processor in "step" when using the execute fault.

- ii) BOS can also be entered by executing an instruction pair located at location 0 or 2 in memory. In this case, the desired address (viz., 0 or 2) is set in switches 0-17 and an execute double (XED) instruction is set in switches 18-35 (the octal value for this is 717200). If the EXECUTE SWITCHES switch is up when the EXECUTE button is pressed, then this XED will be executed: the processor should be in "step" when the button is pressed. BOS should be entered with a XED only in the cases noted below, or as a last resort.

Note: If the GIOC bell rings, the GIOC CLEAR button on the GIOC should be pressed before pressing the EXECUTE button on a processor.

- c. Clock - For the prototype clock, the CONTROL PORT switch must be set to the first CPU in the BOS deck (i.e., the bootload cpu).
 - d. GIOC - Unused memory ports must be set to "OFF".
2. BOS Configuration Deck
- a. Order of deck - The order of cards is important only for CPU and MEM cards. The first CPU card is for the "bootload" CPU. The MEM cards must be in the order of increasing address.
 - b. Special requirements -
 - i) Whenever going from one processor to two processor operation, do a "warm boot" of BOS after the hardware configuration switches have been set up. In anticipation of future reconfiguration capabilities, the current arbitrary naming of the memories should be changed to the names of the active module ports they are physically connected to. All that is needed to do this is to change the names on the BOS configuration cards for memories and clocks. (And, presumably, the names which operations associates with physical modules). This will avoid confusion later (with reconfiguration) when the system attempts to communicate with the operator in terms of active module port name. The following changes are needed:

<u>CURRENT NAME</u>	<u>CHANGE TO</u>
MEM F	MEM B
MEM G	MEM C
MEM H	MEM D
CLOK G	CLOK C

3. Significance of order of memories. With either 256K or 384K, memories can be in any order convenient. However, if interlace is used, the interlaced memories must be low order.
4. Relevance of "unused" hardware. Unused GIOC's and drums should have the port turned OFF for all memories that are in use as part of Multics.
5. Crashes and Shutdown.
 - a. Crashes - If the above instructions are followed, then whenever Multics crashes and BOS is entered either by Multics or manually, the existing dump procedure should be followed. However, with two processors the following changes should be made:
 - i) Do a PROC ALL dump on tape instead of a DUMP W.
 - ii) When through with all the normal (one processor) dumps, just before ESD, read the DSBR from the non-bootload processor maintenance panel (bit numbers 0-17) and give this value to the BOS dumper by typing DBR XXX. Then repeat the on-line dump for REGS, PRDS, PDS, and PDF.
 - iii) If in the unusual event that Multics will not go to BOS, put both processors in "step", transfer to BOS using the XED of zero (i.e., with EXECUTE SWITCHES switch "up" switches 0-17 down 717200 in switches 18-35) on the bootload cpu and take dumps as required but do not put an EOF on tape. When done with dumps put bootload cpu in "step", transfer to BOS using the XED of two (i.e., with EXECUTE SWITCHES switch "up" and switch 16 up) on non-bootload cpu. Then dump REGS on line and on tape. When through

(including EOF on tape), hit INIT on operator console (do not put in "step"). Transfer to BOS using the XED of zero on the bootload cpu, and continue normal crash procedure. The above procedure is done in order to dump the registers of the non-bootload cpu and leave it in a DIS state.

- b. Shutdown - Shutdown, boot, and salvaging are the same regardless of the configuration.

Warning: With two processors, NEVER put either processor in "step" (except in the case Multics cannot get to BOS as in paragraph 5.a.iii above). If processors must be put in step (e.g., for work by the F.E.'s) then, go to BOS with "bos" command using current procedure: put both processors in "step" only while in BOS.

Temporary Note: There is currently a bug in BOS that affects two processor operation, and until fixed the following applies if, and only if a standard (not prototype) clock is used in a memory that is not low order. Before doing a BOOT or SALV, the INIT button on the operators console must be pressed. Then transfer to BOS on the bootload cpu.